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Future Package Technologies for Wireless Communication Systems

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Future Package Technologies for Wireless Communication Systems

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ABSTRACT

In this paper we discuss two package technologies suitable for achieving low-cost small form factor wireless communication systems in the future. First, an embedded passives technology is described with the aim of miniaturizing the form factor of the RF front-end module and baseband power supply by using high-performance inductors, capacitors, resistors, and derivative circuits embedded in the package substrate. Second, a new stacked package architecture for communication and wireless products is described. This package solution enables the integration of high-speed processors and memories in a single package providing excellent signal integrity and high wiring density.

INTRODUCTION

The convergence of computing and communication continues to drive the complexity of future wireless communication systems. Over the last few years, hand-held devices such as cellular phones have evolved from simple voice communication devices to multifunctional (multimedia) devices that can operate on multiple networks (GSM, DCS, PCS, etc.) while providing other functionalities such as computing, photography, video recording, gaming, and music. At the same time, laptop computers with wireless access have seen a drastic increase in demand. Emerging radio architectures such as Multiple Inputs Multiple Outputs (MIMO) are being introduced to improve data transfer rates. These new technologies have added complexities to the traditional wireless device architecture shown in Figure 1, both at the silicon and package level. At the silicon level, multi-band

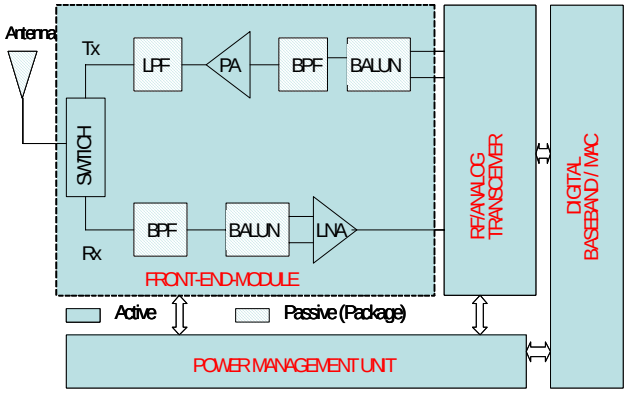


Figure 1: Illustrative block diagram of a single-band wireless communication device

and MIMO radios increase the amount of signal interference and noise vulnerability of the transceiver. The increase in entertainment-based capabilities require more signal processing power, which typically translates into larger die size or multiple dies for the baseband as well as more board-level passive components (especially resistors and capacitors) to sustain the baseband power supply and management. At the package level, introducing multiple radios operating at different frequency bands leads to the need for more or reconfigurable antennas, as well as the evolution of the front-end module from having a single transmit and receive path to having a more complex architecture. This kind of architecture requires several transmit and receive paths with limited interference between them. Besides the complexity of the new wireless architectures, there is constant demand for decreasing the form factor. These challenges are addressed at the package level by developing new affordable and reliable

technologies that not only provide the best performance, but also address the form factor trends and performance per unit volume of the component.

This paper describes two different package technologies to help address the demands on the system in the areas of performance and form factor. In the next section we describe the details of an embedded passives technology that has the potential to replace traditional surface mount passives used in RF Front-End Modules (FEM). Particular emphasis is put on feasibility demonstrations, which include designing, fabricating, and characterizing individual components and major RF passive subcircuits. In the following section, we present a novel stack-package architecture suitable for typical baseband components. This new package architecture provides additional balance between high-speed and high-density interconnects between packages and increases the flexibility of stacking options. Overall, we cover two types of technology options being evaluated to reduce the form factor, increase the integration of components, and provide the capability to mix and match logic and memories.

EMBEDDED PASSIVES TECHNOLOGY FOR MINIATURIZED FRONT-END MODULE AND BASEBAND POWER SUPPLY

Materials Overview and Process

Three types of Embedded Passive (EP) technology are widely discussed in the industry for RF module applications. The first is a Multi-Layer Organic (MLO) substrate, which is built by laminating thick epoxy-based resistor and capacitor films. In this technology, inductors and transmission lines are formed by plating and etching of mostly copper metal. The second type of EP technology is Low Temperature Co-firing Ceramic (LTCC) substrate, which is fabricated by laminating thin ceramic green sheets and co-firing them at temperatures below 1000°C. In this process, inductors and transmission lines are fabricated by screen printing of thick film metal that have a high melting point, such as silver and its alloys, onto the ceramic green sheet. The high dielectric constant (high-k) ceramic green sheets are laminated onto printed metal films to make parallel-plate capacitors. The third technology consists of multi-layer passive thin films that are deposited onto silicon, alumina, quartz, or GaAs substrates. In this technology, Integrated Circuit (IC) materials and processes are typically used to fabricate inductors, resistors, and capacitors. Thus, the smallest form factor can be obtained through this thin-film technology; however it has the disadvantage of being costly and it has some assembly issues.

As an extension of Intel's microprocessor package technology to address future customer demands and market needs, the implementation of laminate EP technology to the multi-layer organic substrate is investigated for wireless module integration. Figure 2 shows the schematic of the cross-sectional view of a typical EP substrate stack-up, where both capacitor and resistor capabilities have been introduced.

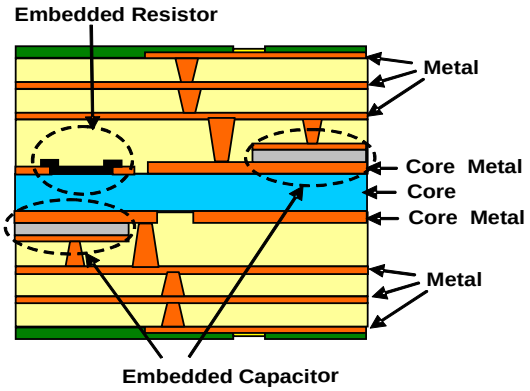


Figure 2: Cross-section of a laminate embedded passive package-stack-up

The integration of passives into the multi-layer organic substrate begins with the lamination of the high permittivity Ceramic Filled Photo-dielectric (CFP) material onto the core metal layer. After drying, sheets of metal are laminated onto the CFP material as top electrodes. Following the patterning of top electrodes through a wet etching process, the CFP is exposed to an UV source while the top electrodes act as a mask. The UV exposed CFP portion is developed and removed to have the final shape of the capacitor structure shown in Figure 2. Following the patterning of the core metal, embedded resistors are formed through screen printing. Transmission line structures such as inductors and baluns are then formed using the standard BGA package technology steps.

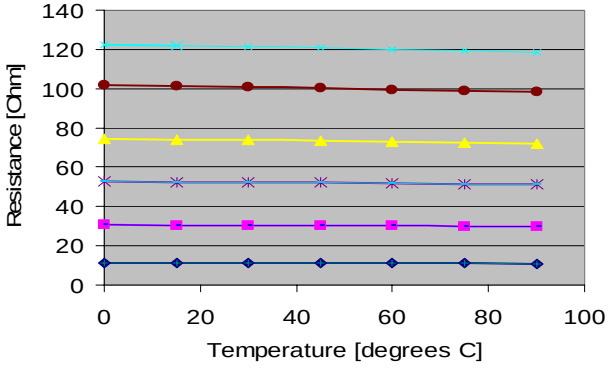
INDIVIDUAL EMBEDDED RF PASSIVE COMPONENTS

Embedded Resistors

The fully embedded resistors were fabricated directly on top of the core substrate. To enable their electrical characterization, the pads are routed to the surface of the package stack-up using multiple layers of vias and interconnections. The final shape of these "rectangular" resistors depends on the process conditions such as temperature and lamination pressure. In the preliminary analysis, resistors were designed to cover the range of 10Ω to 48 kΩ using two inks of different resitivities. The top view of a fabricated resistor is illustrated in Figure 3a.

Embedded resistors are primarily targeting DC power delivery of wireless communication systems. As such they were mainly characterized at very low frequencies. The DC resistance was first evaluated at room temperature using 4-wire resistance measurement techniques. For examining the fabrication process stability, a statistical analysis was also performed by measuring each resistor on 60 different test vehicles. In a second evaluation, the temperature linearity of the resistors was investigated. The temperature was swept from 0 to 90ºC in 15ºC steps. Figure 3b shows the temperature dependency of low-resistance resistors. The overall decrease in resistance with temperature was less than 5%.

(a)



(b)

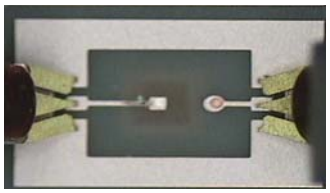
Figure 3: (a) Top view and (b) temperature dependence of embedded resistors

Embedded Capacitors

The capacitors considered in this study are parallel plate capacitors consisting of high k thin film dielectric material sandwiched between two copper electrodes. The parallel-plate capacitor is connected to the surface of the package or to other components using additional interconnects and multilayer vias as illustrated in Figure 2. Capacitors ranging from 0.3 pF to 10 pF were fabricated and characterized. Capacitance values were first estimated using equation (1), which represents the general equation for a typical parallel-plate capacitor.

$$C = \varepsilon_0 \cdot k \cdot \frac{W \cdot L}{d} \qquad (1)$$

In (1), W and L represent the width and length of the top electrode, whereas d is the distance between the parallel electrodes and k is the dielectric constant. Figure 4a illustrates the top view of a typical embedded capacitor fabricated in this technology.



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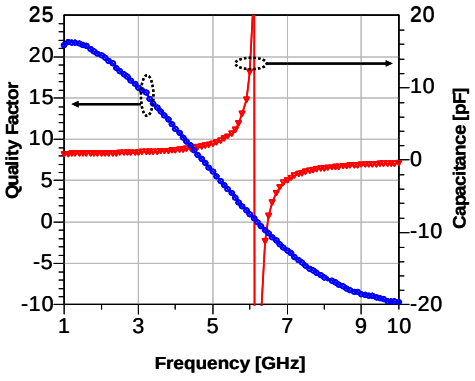


(b)

Figure 4: (a) Top view and (b) measured electrical performance of a 1pF embedded capacitor

The key electrical attributes of the capacitors with respect to the RF applications are the quality factor Q, the capacitance C and the Self Resonance Frequency (SRF) that are extracted from the modeled or measured S-parameters using the methodology reported in [1]. Figure 4b shows the extracted Q and C of a typical 1pF RF capacitor. Most capacitors showed a quality factor of about 18 at 2.4 GHz with a peak value around 25 at lower frequencies. This value is comparable to that of LTCC-embedded capacitors reported in the literature [2] and is slightly lower than the quality factor of silicon-integrated Metal-Insulator-Metal (MIM) capacitors of similar capacitance value [3]. The relatively low SRF of the embedded capacitors can be inferred to the parasitic inductance of both the electrodes and feeding lines used for the RF characterization.

Embedded Inductors

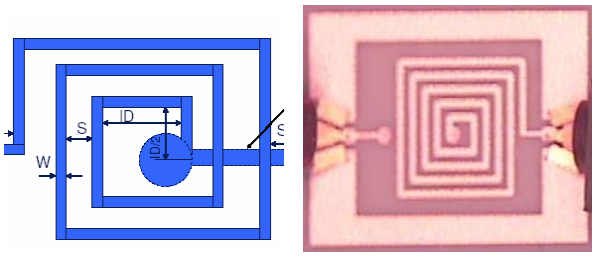
Inductors are one of the critical components for RF designs because of their application in several functionalities such as biasing, matching, filtering, and feedback circuits. As the frequency increases, the requirement on the inductance value decreases. However,

the requirements on the quality factor become even more stringent. In order to replace the traditional discrete filters and matching networks used in the RF modules with integrated LC-based components, it's imperative that the new inductors exhibit extremely high quality factors. Several spiral inductors of interest for wireless communication have been designed to evaluate the embedded passives technology capability. A typical spiral inductor is illustrated in Figure 5a. Its main physical parameters are the trace width (W), the trace spacing (S), the number of turns (N), the inner diameter (ID), and the substrate layer (H) on which the spiral is routed. The number of turns was varied form 1 to 4.5 to cover both nH and sub-nH inductors suitable for the frequency range of interest for Wi-Fi*, WiMax, and UWB. For proper electrical characterization, the inductors were laid out following the guidelines for ground-to-device separation described in [1]. The key performance metrics, which are the inductance L and the quality factor Q, were obtained from the Y-parameters using equations (2) and (3), whereby Y(1,1) is an element of the two-port admittance matrix obtained from the two-port S-parameters using the transformation described in [4]. ω is the angular frequency.

$$Q = -\frac{\mathrm{Im}[Y(1,1)]}{\mathrm{Re}[Y(1,1)]} \qquad (2)$$

$$L = \frac{\mathrm{Im}[1/Y(1,1)]}{\omega} \qquad (3)$$

Quality factors in the order of 50 to 70 were achieved for 1 to 5 nH inductors at frequencies of interest for Wi-Fi and WiMax applications. For example, Figure 5b shows the inductance and quality factor of a 2.8 nH with and without the underlying ground shield. The peak Q value decreases by about 40-50% with a simultaneous decrease in both SRF and effective inductance when the device is subjected to a non-optimized ground shield. Even in the presence of a ground plane, the quality factor is still better than that reported to date for inductors on CMOS or BiCMOS technologies [5]. Package-embedded inductors, as reported in [6], have exhibited a slightly lower quality factor due to an even closer proximity of the ground shield.



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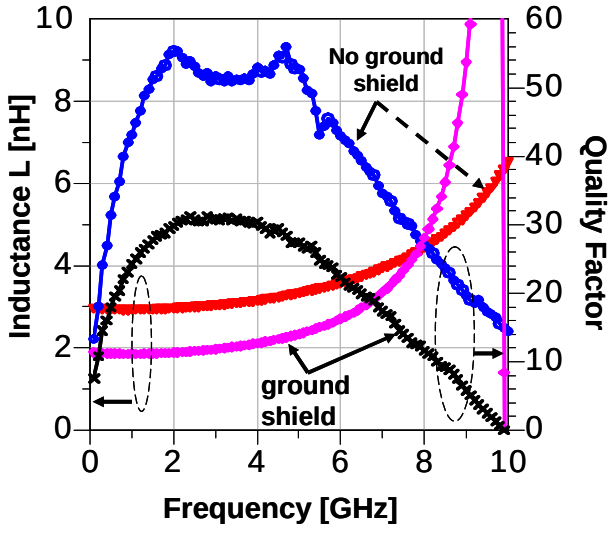

(b)

Figure 5: (a) Top view and (b) measured electrical performance of typical embedded RF inductors with and without ground shield

EMBEDDED RF PASSIVE CIRCUITS– FILTERS, MATCHING NETWORKS AND BALUNS

Overview and Design Flow

The limited space in hand-held/mobile devices has placed more and more critical requirements on the form factor of the RF front-end passive building blocks. The smaller size of the RF passive building blocks will ultimately lower the product cost. Typically, these building blocks include filters (LPF/BPF/BSF), baluns, and matching networks.

Integrated passive circuits can be designed using distributed or lumped elements. While distributed elements are easily achievable in typical PCB and package technologies, the dependence of the circuit elements on the electromagnetic wavelength leads to large area circuits. Designs using lumped element components such as L and C provide both compactness and superior

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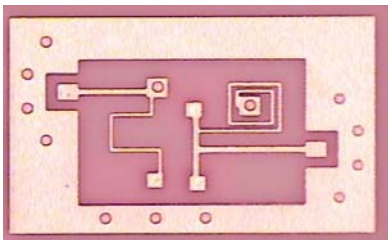
electrical characteristics. Using the embedded passives technology, we designed several filters and matching networks according to the following 3-step design flow: (1) circuit topology determination based on the in-band insertion loss and out-of-band rejection requirement; (2) circuit-level simulation and optimization with finite values of Ls and Cs that reflect the real value of the lumped components as provided by the substrate, and (3) 3D-modeling and layout optimization to accommodate interconnect and component-to-component interaction.

Filter Implementation and Characterization

Several RF filters for WLAN applications have been fabricated and fully characterized. Figure 6 shows the top view and modeled vs. measured electrical performance of a harmonic rejection low-pass filter suitable for application in the transmit path of the WLAN front-end module. This five-element filter includes two embedded inductors and three capacitors. The filter occupies an estimated area of 1.8mmx2.6mm and exhibits an insertion loss of less than 0.5dB in the pass-band with second and third harmonic rejection better than 33 and 45dB, respectively. These electrical performances are similar to or better than those of a similar laminate-based filter reported in [7].



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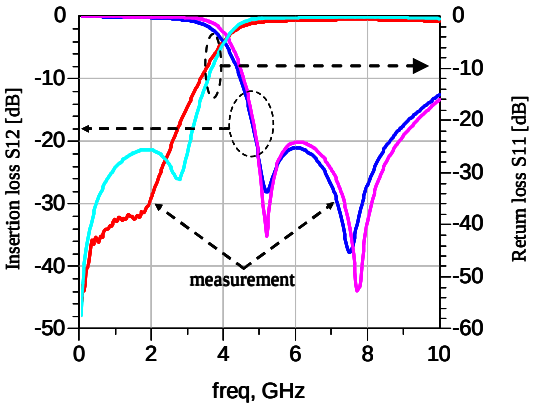


(b)

Figure 6: (a) Top view and (b) electrical performance of package-embedded harmonic rejection low-pass filter; blue and pink are modeled data

The frequency response of a narrowband WLAN band-pass filter, designed for 2.4 GHz applications is shown in Figure 7. More importantly, this filter exhibits high signal rejection at the frequency of interest for WiMax applications, making it suitable for applications in future single-package multiband radios, where Wi-Fi and WiMax have to coexist.

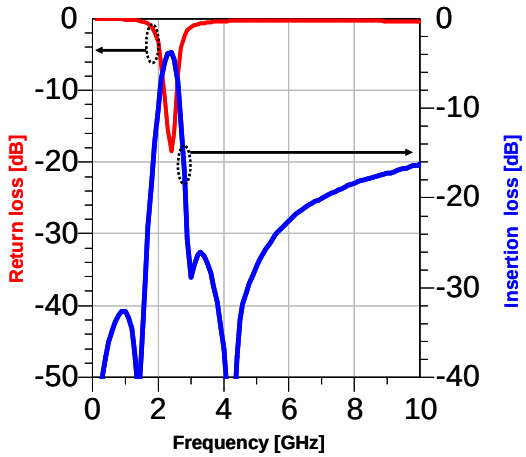


Figure 7: Measured electrical performance of 2.4 GHz band-pass filter

Matching Network Design and Characterization

Matching networks are often used between two different RF components to transform them from one impedance to another, in order to maximize the RF power transfer. They can be found both in Rx path, from VCO to mixer, filter to LNA, and in Tx path, from PA to antenna, etc.

Different topologies of the matching networks, such as T-type and Pi-type, have been investigated in the embedded passives technology using both commercially available and in-house developed design tools. As a design example, Figure 8 shows the frequency response of a differential CMOS Low-Noise Amplifier (LNA) with the input matching network implemented on the package. The matching network has dimensions of 2mmx1.5mm and provides about 5.8dB improvement on the insertion loss (or gain) in comparison to the non-matched circuit.

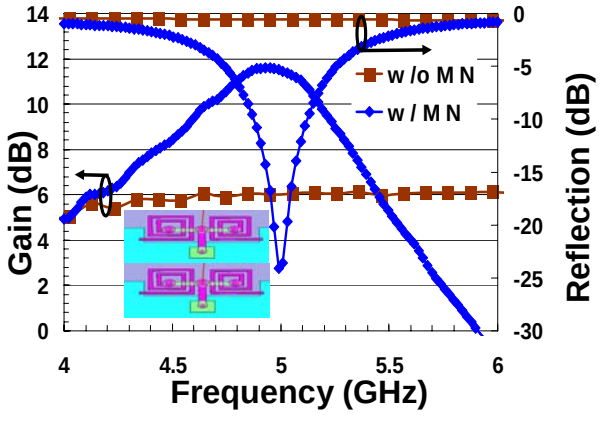


Figure 8: Measured electrical performance of 5 GHz LNA with package-embedded matching network

Embedded Balun Design and Characterization

Baluns are integral components in wireless systems providing balanced outputs from an unbalanced input. Balanced outputs require half the input signal amplitude at the two output terminals, which are 180° out of phase with each other. They are an important component for double-balanced mixers, push-pull amplifiers, and matching between antenna and the RF front end. For passive implementations of RF baluns, there exist several types, such as the 180° hybrid type, the lumped-element filter type, and the Marchand type using a coupled transmission line [8, 9]. Figure 9 shows the 3-D schematic of the balun evaluated in this work. It is a compensated Marchand-type balun in the coiled-up spiral configuration. Due to its increased mutual capacitance and inductance, this spiral configuration balun is very suitable for relatively low-frequency applications, compared to straight line or microstrip line implementation designs.

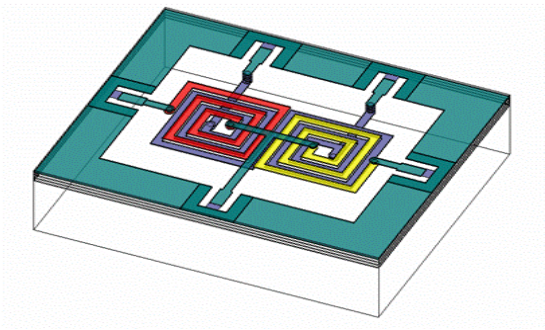
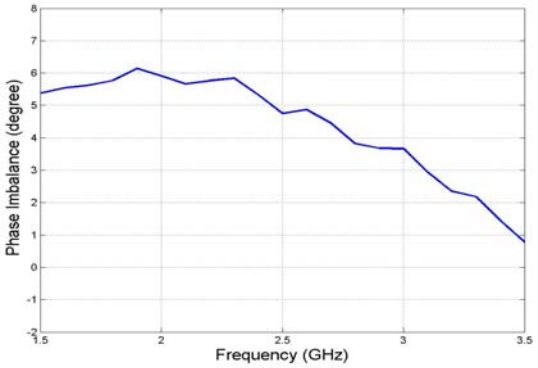
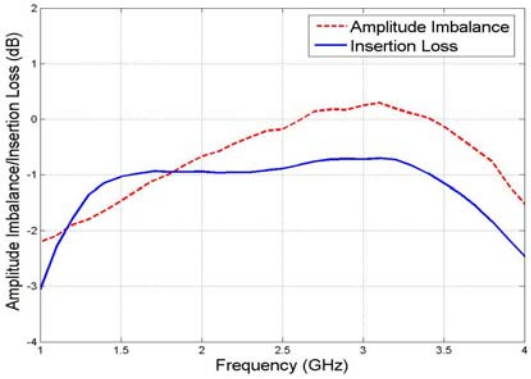


Figure 9: 3-D schematic picture of the implemented spiral Marchand balun

The dimension of the device is 7mmx4mm. The operation frequency of this 50:100Ω balun is 2.4 GHz for Bluetooth and WLAN applications. Figure 10 shows the measured electrical performance of the fabricated device. These data were measured using a 4-port Performance Network Analyzer (PNA). The differential insertion loss, which represents the total power transfer from the input port to the two differential output ports, is less than 1dB in the broad frequency range of 1.8 to 3.4 GHz. The signal difference between the two output ports is characterized by the amplitude imbalance and phase imbalance, which were measured to be less than 1dB and 6° over the wide frequency band of 1.8-3.4 GHz, respectively. These electrical performances are better than most data reported in the literature. Further improvement in performance can be made through a rigorous optimization process in design variables such as inner diameter, trace width, and spacing between traces in the spiral balun geometry.



(a)



(b)

Figure 10: Measured electrical performance of the implemented balun (a) phase imbalance, (b) insertion loss and amplitude imbalance

EMBEDDED PASSIVES CHALLENGES AND DISCUSSION

Laminate EP technology in the PCB industry has a low-cost, simple fabrication process and limited or no assembly issues. However, the reported tolerance of embedded capacitors and resistors on PCB is still around 20%. A laser trimming process has been introduced in the EP industry that has produced embedded resistors with a better than 1% tolerance. Challenges remain for the laminate organic-based capacitor, where the geometry of the structures is a limiting factor for laser trimming. The capacitor, a predominant passive component in most RF front-end designs, should have a tolerance of about 5% for robust SiP applications. This tolerance improvement requires tighter control of process parameters associated with the thickness of the high-k dielectric material and patterning of the electrodes.

While the introduction of embedded passives is a key enabler to miniaturize RF front-end modules for future wireless communication systems, it's critical to note that more and more interactions will occur between the different RF building blocks associated with multimode/multiband, especially as various radio standards are merged in the same package. Furthermore, the proximity between radio bands such as WCDMA and Wi-Fi or Bluetooth will require band-pass filters with sharper roff-offs. The associated EP technology should be able to provide good electrical characteristics in the 25-30 GHz, where higher order harmonics of UWB applications will occur. Achieving this goal will require continuous material development and integration as well as tighter tolerance control in the process.

STACKED PACKAGE-ON-PACKAGE TECHNOLOGY FOR IMPROVED 3D INTEGRATION

Overview and Background

The challenge of System in Package (SIP) technology has several features such as stacking the die with four, five, and more than six dies in a single package [10], integrating processor and memory die into a multi-chip system, and stacking dies in stacked packages [11].

Package-on-package (POP) stacking has become an important feature for Original Equipment Manufacturers (OEMs). The benefits are the potentially smallest package body size, a mix and match logic with multiple memories, and flexibility of assembly. Since individual packages are the known good packages as tested prior to stacking; OEM can stack POP at their site for custom combinations.

There are already some stacked package concepts in the industry; however, we need to continue to look at stacked technologies that meet the emerging demands of the largest number of customers. Not all of the demands of the customer are satisfied by the existing technology. For example, some industry concepts do not have the wiring density needed.

What is proposed in this section is a new package architecture to provide additional balance between high-speed and high-density interconnects between packages and the flexibility of stacking configurations. Figures 11 and 12 show a schematic and cross-sectional photo of this new package concept called Stacked Package-Chip Size Package (SP-CSP).

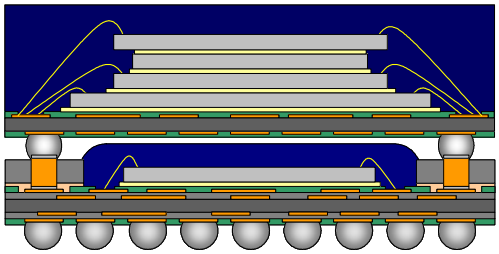


Figure 11: Cross-sectional schematic of SP-CSP

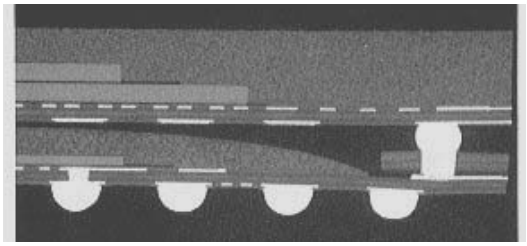


Figure 12: Cross-sectional photo of SP-CSP

In this example two packages are stacked. The top package is a multi-chip package that stacks flash memories and Random Access Memory (RAM). This package is assembled with a conventional process and it is also known as a Matrix Molded Array Package (MMAP). The bottom package is a single chip package and it assumes packaging some logic chip. On the front side of the bottom package, there are land pads placed at the package's peripheral through an intermediate substrate called an interposer. These land pads are used for electrical communication between the top and bottom packages by mounting the top package on them. Three-package stacking is also available as long as the total package height meets the product segment's requirements. A beneficial feature of this package solution is each individual package can be tested as a Ball Grid Array (BGA) package before it is stacked. In other words, the known good package can be selectively integrated for final assembly. The other advantage of this package solution is that proven assembly technology can be leveraged.

Materials and Methods

The interposer that interconnects top and bottom packages is the key building block technology to realize this concept. The vertical interconnects must be high density, but require the stand-off height to assemble one or two dies in the bottom package. Thus, it requires a higher aspect ratio of z-directional connection than a conventional solder ball interconnect.

Figures 13 and 14 show the schematic diagram and SEM photograph of the developed interconnect structure [12]. The copper columns are implanted into a glass woven resin core substrate and then laminated on the bottom package substrate by a vacuumed hot press. After assembling the top and bottom packages, an interconnection is made by a solder ball reflow process to mate both packages. The minimum interconnection pitch demonstrated was a 0.33mm pitch at a total of 160 interconnects with a single row peripheral pad. 330 interconnects with dual rows in a 14 x 14mm package can be achieved.

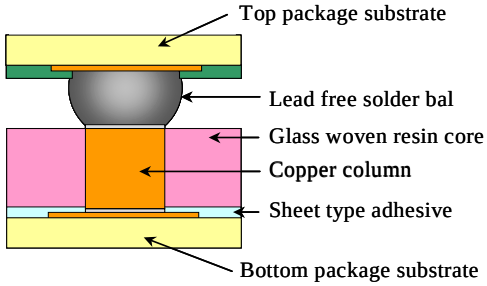


Figure 13: Schematic diagram of solder ball, reflow bonding structure with a copper column implanted interposer

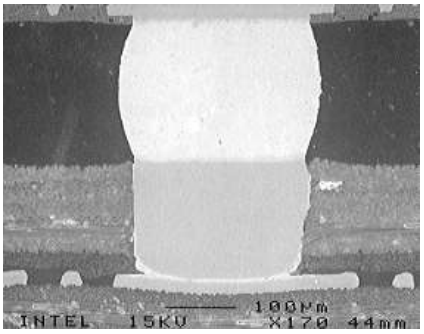


Figure 14: SEM photo of solder ball reflow bonding using a copper column implanted interposer

Results

Table 1 and 2 summarize the results of reliability testing [13]. It was very encouraging even though the sample size is not large enough for a final conclusion. There were no electrical failures detected during the stress test. The remarkable point of these stress test results is not only for BGA, but also for the package-to-package interconnect solder joint reliability. SP-CSP showed a very resilient solder joint reliability performance even in the absence of underfill material

Table 1: Unit-level reliability testing

Stress	Results
MSL3 Preconditioning (7 hrs bake@125˚C, 5x T/C 'B', 216hrs 30˚C/60%RH + 3x CR @ peak temp of 260˚C)	0 / 30 unit fail
MSL3 + T/C 'B' 1000 cycles (-55˚C to 125˚C)	0 / 20 unit fail
MSL3 + Biased HAST 100 hrs (130˚C/85%RH, +3.3V)	0 / 10 unit fail
Bake @ 150˚C, 500 hours	0 / 10 unit fail

Table 2: Second-level board reliability testing

Stress	Results
T/C 'G' 2500 cycles (-40˚C to 125˚C)	0 / 30 unit fail
Drop 250 drops (1500G/0.5ms/half sine pulse , Z-axis)	0 / 27 unit fail
3 point Board Bend (5 & 6.5mm displacement, 1.25Hz)	>100K cycles at 0.001 strain

Thermo-Mechanical Stress

Interposer and substrate joint reliability were evaluated by a temperature cycle test with Level-3 preconditioning. Figure 15 shows the electrical joint resistance of a copper plug and substrate pad. The joint resistances were not changed throughout the temperature cycle, and they didn't increase even after 1000 'B' condition temperature cycles.

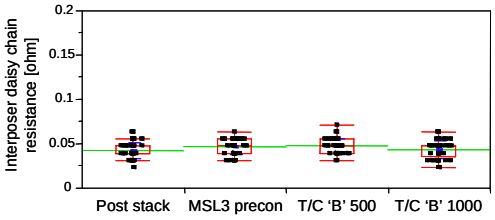


Figure 15: Copper plug/substrate pad tin joint daisy chain resistance change by thermal cycle

Moisture Stress and Ion Migration

Package integrity with regard to moisture sensitivity and metal ion migration was evaluated by biased HAST with preconditioning. A voltage of 3.3 volts was applied to every other package-to-package interconnection solder ball. No leakage current was measured. Moreover, tin and copper migrations were not detected by Energy Dispersive X-ray analysis (EDX).

High-Temperature Storage

A high-temperature storage test was performed to investigate the effect of the growth of the inter-metallic compound. Figure 16 is the cross-sectional SEM image of a tin joint between a copper plug and a nickel-gold finished substrate pad after 500 hours storage at 150˚C constant temperature. A thin inter-metallic layer in between the copper and tin was observed. The main concern had been the breakdown of the tin joint because of the brittleness of the inter-metallic compound. However, inter-metallic growth was not observed even after 1000 hours.

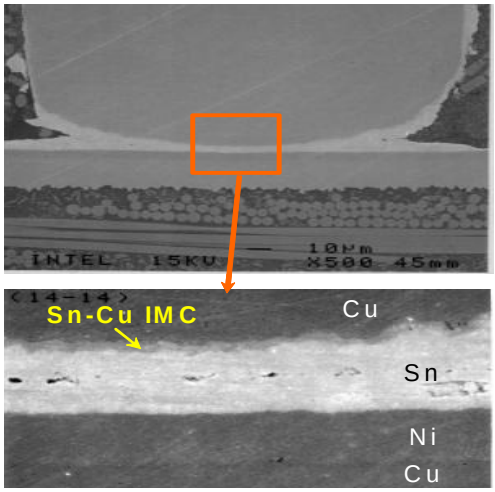


Figure 16: Cross-sectional SEM image of copper plug tin joint

Signal Integrity

The potential problem of electrical performance in stacked packages is the power delivery due to loop inductance from the BGA to the top package. Another problem is cross-talk among signal traces due to highly scrambled routing between the packages. As a result of electrical modeling (see Table 3), it was found that excellent signal integrity can be maintained and SP-CSP will be able to meet future product segment requirements of power delivery and cross-talk even at higher bus speeds. Ground planes of the top package substrate are helping to reduce cross-talk by allowing a micro-strip line structure. In addition, SP-CSP can route a signal with a short trace length because routing is possible from any edge of the package. This helped to reduce loop inductance a lot.

Table 3: Electrical performance

Attribute	SP-CSP
I/O Power Delivery	Meet
Cross-Talk	Meet

Discussion

Package Design Integration

SP-CSP is able to make the electrical connection between top and bottom packages at any side of the package

peripheral. This structural advantage offers high routing flexibility, and loop inductance can be controlled to a small value. As a result, a high-speed bus between the processor and memories can be designed. This is the major advantage of this package.

Figure 17 shows a case example of designing and manufacturing a functional engineering sample with an SP-CSP package platform using actual processor and flash memory dies to verify the feasibility of signal routing. The package size was 13 x 13mm, and it has a 96 pin package-to-package interconnection with a 0.5mm pitch.

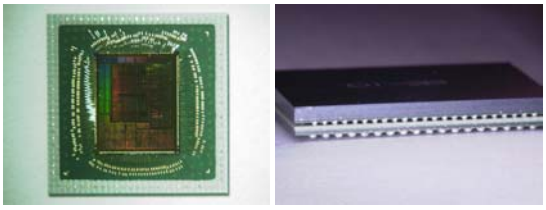


Figure 17. Appearance of the functional engineering sample of a processor and memory stacked package (Left: bottom of package, processor die is not encapsulated. Right: Stacked package)

Figure 18a and 18b shows a case that achieved a 160 pin interconnect with a single row pad at a 14 x 14mm package peripheral by reducing the package-to-package interconnection pitch from 0.5mm to 0.33mm.

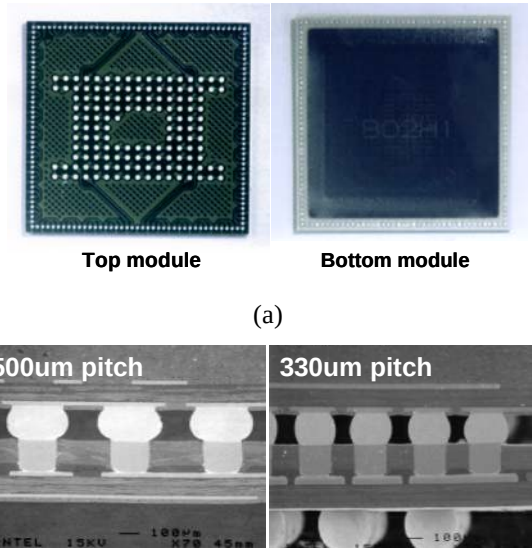


Figure 18: (a) Appearance of test vehicle for 0.33mm pitch package-to-package interconnection and (b) cross-sectional SEM image of package-to-package interconnection

Even though a 0.33mm pitch BGA is available, its test process is very difficult with current technology in terms of socket equipment and automation. Since a test before package stacking is one of the major advantages of SP-CSP, this is a critical problem. There is a potential solution to this problem. Test pads are placed with a 0.8mm pitch Land Grid Array (LGA) in the central area as shown in Figure 8a. It is possible to test the top package without probing the 0.33mm pitch BGA with these LGA pads by using legacy test equipment.

Embedded Logic Die in Package

The original concept of an SP-CSP stacked package has pads at the perimeter of the package. This concept requires a customized top package with perimeter pads for SP-CSP and is hence not compatible with off-the-shelf memory products. Since this constraint may make it difficult to create a business model, we have extended the package concept so that the standard memory package with area array pads can be stacked. Figure 19 shows the cross-sectional schematic of the logic die embedded in the bottom package.

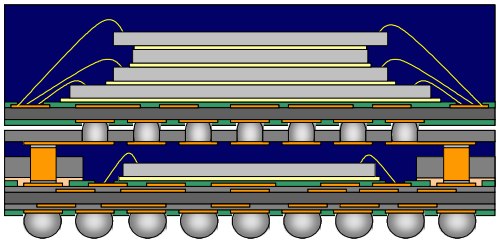


Figure 19: Schematic of a die embedded bottom package architecture for standard memory package stacking

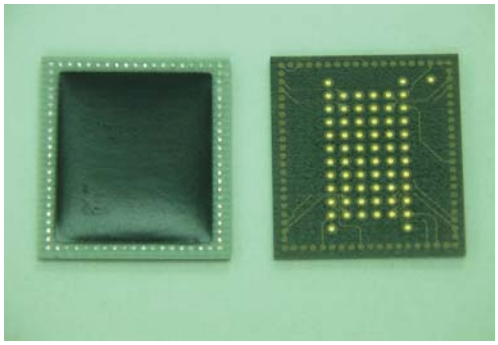


Figure 20: Top view of the perimeter pads, original concept (left) and the array pads extended concept with die embedded (right)

In this concept, a single-sided substrate is laminated as the re-distribution layer for the bottom package by using a thermo-compression bonding technique. The differences in the package's appearance between the original architecture are shown in Figure 20. A single-layer substrate is used in the schematic, but a 2-metal layer substrate is also applicable to make a micro strip line structure or high-density re-distribution.

CONCLUSION

The current BGA multilayer organic substrate process, which is very mature for Intel's microprocessor packages, has been extended to include an embedded passives technology capability. Several inductors, that exhibit superior electrical performance, as well as embedded capacitors and resistors have been fabricated and fully characterized. Using WLAN/Wi-Fi as a reference, we successfully demonstrated the integration of all RF passive building blocks for a 2.4/5 GHz WLAN module, which includes baluns, matching networks, diplexers, and filters. These exhibit exceptional electrical performance and occupy very small real estate. Limited statistical analysis has been performed on selected structures to confirm the stability of the embedded passives process for high-volume manufacturability. With the aim of further miniaturizing the non-RF aspect of wireless communication packages, we also introduced a new stacked package solution. We proved that an SP-CSP package platform can be a promising solution for future multi-chip stacked products. It offers excellent signal integrity and a highly flexible signal routing design capability with a reliable package. These two technologies are only two among several package solutions being pursued for future wireless communication needs.

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